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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes

Title: SILICON-GERMANIUM DEVICES FOR CMOS FORMED BY ION IMPLANTATION AND SOLID PHASE EPITAXIAL REGROWTH

Docket No.: 303.229US2
Filed: August 11, 1998
Examiner: Mark V. Prenty

Serial No.: 09/132,157
Due Date: December 9, 2002
Group Art Unit: 2822

Box AF
Commissioner for Patents
Washington, D.C. 20231

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S/N 09/132,157 **PATENT**

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36 Appeal Brief 12-19-02

APPEAL BRIEF TO THE BOARD OF PATENT APPEALS AND INTERFERENCES OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Sir:

Appellant's Brief on Appeal

This Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences filed concurrently on October 9, 2002, from the Final Rejection of claims 11, 13, 14, 24-28, 32, and 38-43 of the above-identified application, as set forth in the Final Office Action mailed July 9, 2002.

This Appeal Brief is filed in triplicate and accompanied by the requisite fee set forth in 37 C.F.R. § 1.17(f). Applicant respectfully requests reversal of the Examiner's rejection of pending claims 11, 13, 14, 24-28, 32, and 38-43.

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APPELLANTS' BRIEF ON APPEAL

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, Micron Technology, Inc., a Delaware corporation doing business at 8000 South Federal Way, P.O. Box 6, Boise, Idaho 83707-0006.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to the Applicant which will have a bearing on the Board's decision in the present appeal.

3. STATUS OF THE CLAIMS

Claims 11, 13, 14, 24-28, 32, and 38-43 are pending, and claims 11, 13, 14, 24-28, 32, and 38-43 are the subject of the present appeal (see Appendix 1).

4. STATUS OF AMENDMENTS

This application was originally filed on August 11, 1998, as a divisional application of Serial number 08/717198, filed September 18, 1996, now U.S. patent number 5,879,996. The present application elected claims 11-14 of the parent case.

In a Preliminary Amendment, mailed on September 29, 1998, claims 24-37 were added.

In the First Office Action mailed October 27, 1998, claims 11-14 were rejected under 35 U.S.C. §102(b) as anticipated by Selvakumar (US Pat. No. 5,426,069).

In the response to the preliminary amendment of September 29, 1998, a supplemental First Office Action mailed December 15, 1998, rejected a number the newly submitted claims over the Selvakumar reference.

In the Amendment and response to the First Office Action, mailed March 15, 1999, claims 11, 24-28, 30, 32, and 33 were amended.

In the Final Office Action mailed May 28, 1999, claims were rejected over the Selvakumar reference.

In a preliminary amendment with a CPA filed on August 11, 1999, claims 33-37 were cancelled, and claims 11, 24-25, 28, and 30 were amended.

In the First Office Action mailed September 1, 1999, claims were rejected over the Selvakumar reference.

In the Amendment and Response to the First Office Action, mailed November 30, 1999, claims 38-43 were added.

In the Final Office Action mailed February 2, 2000, claims were rejected over the Selvakumar reference.

In a Preliminary Amendment with a CPA filed on June 30, 2000, claims 11, 24, 25, 28, 30, 38, 40, and 41 were amended and claims 12 and 29 were cancelled.

In the First Office Action mailed July 18, 2000, claims were rejected over the Selvakumar reference.

In the Amendment and Response to the First Office Action, mailed October 18, 2000, claims 11, 24, 25, 28, 30, 38, and 40 were amended.

In the Final Office Action mailed October 30, 2000, claims were rejected over the Selvakumar reference.

In the Amendment and Response to the Final Office Action mailed on December 22, 2000, claims 11, 24, 25, 28, 32, 38, 40, 41 and 43 were amended and claims 30-31 were cancelled.

An RCE was filed on January 29, 2001 to enter the Amendment and Response to the Final Office Action.

In the First Office Action mailed June 7, 2001, claims were rejected over the Selvakumar reference.

In the Amendment and Response to the First Office Action, mailed September 7, 2001, claims 11, 24, 25, 28, 30, 38, and 40 were amended.

In the Final Office Action mailed September 25, 2001, claims were rejected over the Selvakumar reference.

In the Amendment and Response to the Final Office Action mailed on November 27, 2001, claims 11, 24, 25, 28, 38, 40, and 41 were amended.

An RCE was filed on December 18, 2001 to enter the Amendment and Response to the Final Office Action.

In the First Office Action mailed February 26, 2002, claims 11, 13, 14, 24-28, 32, and 38-43 were rejected over the Selvakumar reference. Claims 11, 13, 14, 24-28, 32, and 38-43 were also rejected over the Nakagawa reference (US Pat. No. 5,272,365).

In the Amendment and Response to the First Office Action, mailed May 28, 2002, no claims were amended.

In the Final Office Action mailed July 9, 2002, claims 11, 13, 14, 24-28, 32, and 38-43 were rejected over the Selvakumar reference.

A notice of appeal was filed on November 9, 2002.

5. SUMMARY OF THE INVENTION

The present invention teaches a method and apparatus for large volume manufacturing of Si-Ge complementary metal-oxide-semiconductor (CMOS) integrated circuits (ICs). $Si_{1-x}Ge_x$ is formed under existing gate oxide layers, eliminating the problem of forming stable gate oxides directly over a $Si_{1-x}Ge_x$ layer. A high dose Ge layer is implanted under the gate oxide layer. Next, a $Si_{1-x}Ge_x$ layer is grown by solid phase epitaxial (SPE) regrowth, such that lattice mismatch is minimized between the $Si_{1-x}Ge_x$ layer and the underlying Si substrate. SPE is performed in a low temperature furnace, for approximately ten minutes. Implantation and anneal steps are commonplace in the large volume manufacture of CMOS ICs. Thus, this invention does not add significant cost or complexity to the manufacture of CMOS ICs, while providing the ability to manufacture high volume CMOS ICs with enhanced field effect hole mobility.

According to one aspect of the invention, the $Si_{1-x}Ge_x$ layer formed in this invention has a critical layer thickness, which depends on the molar fraction, x, of germanium present in the $Si_{1-x}Ge_x$ compound formed. As long as the critical layer thickness is not exceeded, $Si_{1-x}Ge_x$ will form defect-free during SPE regrowth. By forming p-channels in accordance with the method of the invention, valuable chip space is conserved, enabling high density chips to be formed. P-channel transistors are able to be formed in approximately the same amount of space as n-channel transistors due to the increased field effect hole mobility, while obtaining symmetrical switching and driving capabilities.

6. ISSUES PRESENTED FOR REVIEW

Whether the Selvakumar reference teaches a $Si_{1-x}Ge_x$ channel region located underneath a SiO_2 gate oxide that possesses both of the following characteristics:

A. a $Si_{1-x}Ge_x/SiO_2$ channel region with a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface; and

B. a $Si_{1-x}Ge_x$ channel region with no germanium oxide present at the $Si_{1-x}Ge_x/SiO_2$ interface.

7. GROUPING OF CLAIMS

Claims 11, 13, 14, 24-28, 32, and 38-43 are to be considered together for purposes of this appeal. The claims stand or fall together.

8. ARGUMENT

The devices shown in the Selvakumar reference, and the products produced by the processes taught in Selvakumar cannot include a SiGe region with both:

A. a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface; and

B. no germanium oxide present at the $Si_{1-x}Ge_x/SiO_2$ interface.

Claims 11, 14, 24, 28, 38, and 40 were rejected under 35 USC § 102(b) as being anticipated by Selvakumar et al. (U.S. Pat. No. 5,426,069). Claims 25, 32, and 41 were rejected under 35 USC § 102(b) as being anticipated by, or in the alternative under 35 USC § 103(a) as obvious over Selvakumar et al. (U.S. Pat. No. 5,426,069).

The Office Action mailed February 26, 2002 states (on page 2, second paragraph, among other locations) that the $Si_{1-x}Ge_x/SiO_2$ region of Selvakumar "forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

The process used by the Selvakumar reference implants germanium (Ge) atoms in the channel region before oxidizing to form a gate oxide. The process of forming the gate oxide in Selvakumar is described in Col. 3, lines 40-68, and in Col. 4, lines 1-3. The description in Selvakumar appears to include first implanting germanium through an exposed window (Col. 3, lines 41-44), then forming a dry gate oxide (Col 3, lines 45-48). Forming the dry oxide is further described as being performed at 1100° C for 50 minutes in dry oxygen and a 20 minute nitrogen anneal.

Applicant submits that, depending on the process conditions of the ion implantation, the ion implantation process either leaves the Ge atoms exposed at the surface to be oxidized, or it buries the Ge atoms in the substrate beneath the surface to be oxidized. The Selvakumar reference is silent as to depth of implanted Ge atoms. Applicant submits that in either case, the product formed by the described process in Selvakumar cannot produce a SiGe region with both: a continuous SiGe/SiO2 gate oxide interface; and no germanium oxide present at the SiGe/SiO2 interface.

If the implanted Ge atoms are buried, then by definition, an intermediate silicon layer exists between the channel surface to be oxidized and the implanted Ge atoms. A continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface is impossible due to the intermediate layer of silicon.

If the implanted Ge atoms are exposed on the surface to be oxidized, Applicant submits that one skilled in the art will recognize that using the oxidation process of Selvakumar as described above, germanium oxide will necessarily be created at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface. Germanium oxides are undesirable because they are not stable, as discussed on page 2, lines 16-19 of Applicant's specification.

In contrast, devices as claimed by Applicant, and products produced by the process claimed by Applicant include a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface. Applicant's unique process implants the germanium after the gate oxide has been formed. The implant of germanium atoms in Applicant's process is directed through the gate oxide, and forms a $Si_{1-x}Ge_x$ channel region and a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface. No oxidation steps are performed in Applicant's process subsequent to the germanium being introduced to the channel region.

The process of Applicant's invention therefore leads to a unique structure implied by the process recited in the claims. No germanium oxide will be formed at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface formed in Applicant's invention because the germanium in Applicant's process is never exposed to an oxidation step. As noted above, germanium oxides are undesirable because they are not stable, as discussed on page 2, lines 16-19 of Applicant's specification.

Applicant respectfully submits that none of the additional references submitted cure these deficiencies of the Selvakumar reference as stated above.

9. SUMMARY

Because the Selvakumar reference does not show every element of Applicant's independent claims, a 35 USC § 102(b) rejection is not supported. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claims 11, 24, 25, 28, 38, 40, and 41. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to the remaining claims that depend therefrom as depending on allowable base claims.

Please charge in the amount of 300.00 and any additional required fees to Deposit Account 19-0743 to cover the filing fee of the Appeal Brief.

Respectfully submitted,

STEPHEN R. PORTER ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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Date 12-9-02 By [signature]

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Reg. No. 47,857

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Tina Kohout
Name

[signature]
Signature

APPENDIX I

The Claims on Appeal

11. A p-channel metal-oxide-semiconductor transistor, comprising:

a silicon substrate;

a silicon dioxide (SiO_2) gate oxide, coupled to the substrate;

a gate, coupled to the SiO_2 gate oxide;

source/drain regions formed in the substrate on opposite sides of the gate; and

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction x, located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface as a result of ion implantation of germanium through the previously formed SiO_2 gate oxide.

13. The transistor of claim 11, wherein the $Si_{1-x}Ge_x$ channel is approximately 100 to 1,000 angstroms thick.

14. The transistor of claim 11, wherein the molar fraction of germanium is approximately 0.2.

24. A p-channel metal-oxide-semiconductor transistor formed on a silicon substrate, comprising:

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region;

wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface as a result of ion implantation of germanium through the previously formed SiO_2 gate oxide.

25. A p-channel metal-oxide-semiconductor transistor formed on a silicon substrate, comprising:

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface as a result of ion implantation of germanium through the previously formed SiO_2 gate oxide; and

wherein the $Si_{1-x}Ge_x$ channel region is formed from ion implanting germanium (Ge) into the substrate at a dose of approximately 2×10^{16} atoms/cm^2, and wherein the Ge is implanted at an energy of approximately 20 to 100 keV.

26. The transistor of claim 24, wherein the Ge is dispersed in the substrate to a depth of approximately 100 to 1,000 angstroms.

27. The transistor of claim 24, wherein the Ge is dispersed in the substrate to a depth of approximately 300 angstroms.

28. A p-channel metal-oxide-semiconductor transistor formed on a silicon substrate, comprising:

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of 0.2, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region, wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface as a result of ion implantation of germanium through the previously formed SiO_2 gate oxide.

32. The transistor of claim 28, wherein, the $Si_{1-x}Ge_x$ channel region was formed by a process comprising:

ion implanting Ge ions through the gate oxide on the substrate at a dose of approximately 2×10^{16} atoms/cm^2, and wherein the Ge was implanted at an energy of approximately 20 to 100 keV; and

annealing the substrate in a furnace at a temperature of approximately 450 to 700 degrees Celsius.

38. A semiconductor transistor, comprising:

a silicon substrate;

a silicon dioxide (SiO_2) gate oxide, coupled to the substrate;

a gate, coupled to the SiO_2 gate oxide;

source/drain regions formed in the substrate on opposite sides of the gate; and

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and located underneath the SiO_2 gate oxide and between the source/drain regions, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface as a result of ion implantation of germanium through the previously formed SiO_2 gate oxide.

39. The transistor of claim 38, wherein the $Si_{1-x}Ge_x$ channel is approximately 100 to 1,000 angstroms thick.

40. A semiconductor transistor formed on a silicon substrate, comprising:

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of 0.2 formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region, wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface as a result of ion implantation of germanium through the previously formed SiO_2 gate oxide.

41. A semiconductor transistor formed on a silicon substrate, comprising:

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction of x, and formed in the substrate, underneath a silicon dioxide (SiO_2) gate oxide and between a source region and a drain region, wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a continuous $Si_{1-x}Ge_x/SiO_2$ gate oxide interface wherein no germanium oxide is present at the $Si_{1-x}Ge_x/SiO_2$ gate oxide interface as a result of ion implantation of germanium through the previously formed SiO_2 gate oxide; and

wherein the $Si_{1-x}Ge_x$ channel region is formed from ion implanting germanium (Ge) into the substrate at a dose of approximately 2 X 10^{16} atoms/cm^2, and wherein the Ge is implanted at an energy of approximately 20 to 100 keV.

43. The transistor of claim 41, wherein the Ge is dispersed in the substrate to a depth of approximately 300 angstroms and the germanium molar fraction is about 0.4.